

# Lock in Amplifier on LabVIEW FPGA

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## REQUIREMENTS:

Application Software: LabVIEW Professional Development System Driver Software: NI-RIO 2.4 Hardware Family: CompactRIO Add-on Software: LabVIEW FPGA Module 8.5 Development Topic: Advanced Signal Processing

Lock-in Amplifier is an instrument that can detect the amplitude and phase of sinusoidal signal with known frequency in extremely low signal to noise environment. This example shows how to use LabVIEW FPGA to build a lock-in amplifier on CompactRIO. The following diagram illustrates the principle of Lock-in Amplifier. A Phase Locked Loop (PLL) will lock to the frequency in the reference channel and generate clean sinusoidal wave. It then multiplies the signal in the mixer, modulating the weak sinusoidal wave in signal channel to DC frequency. After a low pass filter, the amplitude and phase of weak sinusoidal wave can be revealed. In this example, PLL, mixer and low pass filter are implemented by LabVIEW FPGA. The performance of FPGA based lock-in amplifier can be summarized below:

Hardware	cRIO 9104 NI 9233
Resolution	24 bit
Sampling Rate	50kHz, limited by 9233
Time Constant	1ms to 20ks
Filter Rolloff	20dB, 40dB, 60dB, 80dB
Noise Level	&lt;-100dB, determined by 9233
Dynamic Reserve	&gt;100dB

For detailed description on the principle of lock-in amplifier, see Principle of Lock in amplifier.pdf in attached file. For detailed description on how to setup the example, including hardware and software requirements, see LIA\_IPnet\_Readme.pdf in attached file. A simplified version of Lock-in Amplifier is also available on the Xilinx academic SPARTAN 3E XUP Board. Please

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